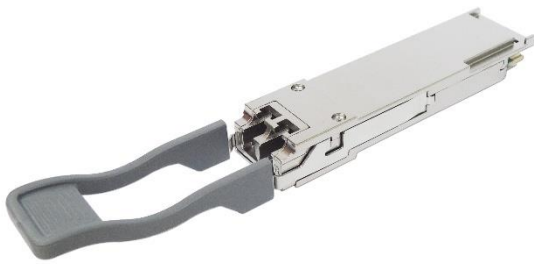




100G QSFP28 SWDM4 Transceiver

Hot Pluggable, Duplex LC, SWDM VCSEL, MMF OM4 100M, DDM

Part Number: FQ28-K7-S85-X1D



Overview

FQ28-K7-S85-X1D is a 4-Channel SWDM QSFP28 transceiver for 100GbE links over in duplex MMF. The transmitter converts 4-Channel 25G electrical input data to four short wavelength optical signals and multiplex that into one 100G signal. The receiver de-multiplex the 100G signal reversely and converts that to 4-Channel 25G electrical output data. The techniques bring a compact transceiver module for an aggregate bandwidth of 100Gbps up to MMF OM4 100m optical links.

Applications

- 100GBASE Ethernet over duplex MMF
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

Features

- Compliant with 100GBASE-SWDM4
- Compliant with SFF-8665 QSFP28 MSA
- Compliant with IEEE 802.3bm CAUI-4 Interface
- 4CH SWDM MUX / DEMUX design
- Supports 103.1Gbps aggregate bit rate
- Hot Pluggable
- 4x25Gb/s VCSEL SWDM transmitter
- Duplex LC connector
- 2-wire interface for management and diagnostic monitor compliant with SFF-8436, SFF-8636
- Single 3.3V power supply
- Link distance 75m over OM3 fiber, 100m over MM OM4 fiber and 150m over OM5 fiber.
- Maximum Power consumption 3.5W
- RoHS compliant

Laser Safety

- This is a Class 1 Laser Product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution: Use of control or adjustments or performance of procedure other than those specified herein may result in hazardous radiation exposure.



Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T _{ST}	-40	+85	°C
Storage Relative Humidity	RH	15	85	%
Supply Voltage	V _{CC}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T _{OP}	0	-	+70	°C
Supply Voltage	V _{CC}	+3.13	+3.3	+3.47	V
Data Rate, per lane	DR		25.78125		Gb/s
Data Rate Accuracy	ΔDR	-100		+100	ppm
Pre-FEC Bit Error Rate	BER			5x10 ⁻⁵	
Supply Current	I _{CC}			1000	mA
Power Consumption	P			3.5	W
Transceiver Power-on Initialization Time				2000	ms
Control Input Voltage High	V _{IH}	2.0		V _{CC}	V
Control Input Voltage Low	V _{IL}	GND		0.8	V
Control Output Voltage High	V _{OH}	2.0		V _{CC}	V
Control Output Voltage Low	V _{OL}	GND		0.8	V



Transmitter Electro-optical Characteristics

$V_{CC} = 3.13V$ to $3.47V$, $T_{OP} = 0\text{ }^{\circ}C$ to $70\text{ }^{\circ}C$

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Lane	DR		25.78125		Gb/s	
Total Average Launch Power	TP_{AVG}	-1.5		+9.0	dBm	
Average Launch Power, per Lane	P_{AVG}	-7.5		+3.0	dBm	
Optical Modulation Amplitude (OMA), per lane	P_{OMA}	-5.5		+3.0	dBm	1
Difference in Launch Power between any two Lanes (OMA)	$P_{TX-DIFF}$			4.5	dB	
Launch Power in OMA minus TDEC, per Lane	OMA-TDEC	-7.7			dB	
Transmitter and Dispersion Eye Closure	TDEC			4.8	dB	
Optical Wavelength, each Lane	λ_{L0}	844	850	858	nm	
	λ_{L1}	874	880	888	nm	
	λ_{L2}	904	910	918	nm	
	λ_{L3}	934	940	948	nm	
Spectral Width (RMS)	$\Delta\lambda$			0.59	nm	1
Optical Extinction Ratio	ER	2.0			dB	
Optical Eye Mask { X1, X2, X3, Y1, Y2, Y3 }		{ 0.3, 0.38, 0.45, 0.35, 0.41, 0.5 }				
Average Launch Power OFF, per Lane	P_{OFF}			-30	dBm	
Relative Intensity Noise	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	ORLT	12			dB	
Input Differential Impedance	Z_{IN}	90	100	110	Ω	
Differential Data Input Voltage	V_{IN-PP}	120		1200	mVpp	

Note1: Transmitter wavelength and launch power need to meet the OMA minus TDP specs to guarantee link performance.



Receiver Electro-optical Characteristics

$V_{CC} = 3.13V$ to $3.47V$, $T_{OP} = 0\text{ }^{\circ}C$ to $70\text{ }^{\circ}C$

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Lane	DR		25.78125		Gb/s	
Damage Threshold, per Lane	D _{TH}	+4.4			dBm	1
Average Receive Power, per Lane	P _{RX-AVG}	-9.5		+3.4	dBm	
Receiver Power (OMA), per Lane	P _{RX-OMA}			+3.0	dBm	
Receiver Sensitivity (OMA), per Lane	SEN _{OMA}			-8.2	dBm	
Stressed Receiver Sensitivity (OMA), per Lane	SEN _{SOMA}			-5.2	dBm	2
Receiver Reflectance	R _{RX}			-12	dB	
LOS De-Assert	LOS _D			-11	dBm	
LOS Assert	LOS _A	-30			dBm	
LOS Hysteresis	LOS _{HY}	0.5			dB	
Output Differential Impedance	Z _{OUT}	90	100	110	Ω	
Differential Data Output Voltage	V _{OUT-PP}	100		1200	mVpp	

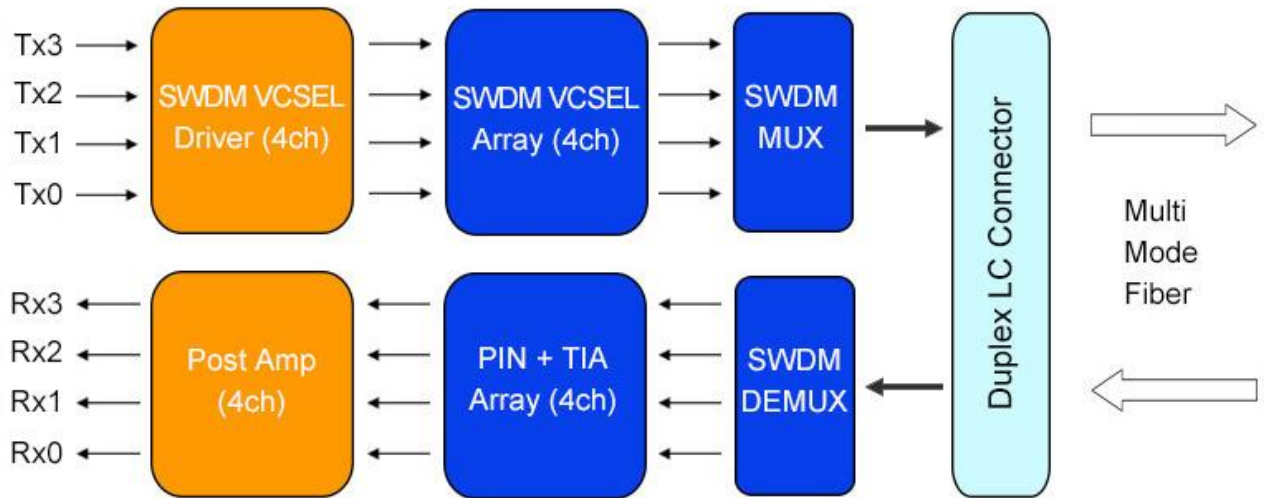
Note1: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Note2: Measured with conformance test signal at receiver input for BER= 5×10^{-5} (Pre-FEC).

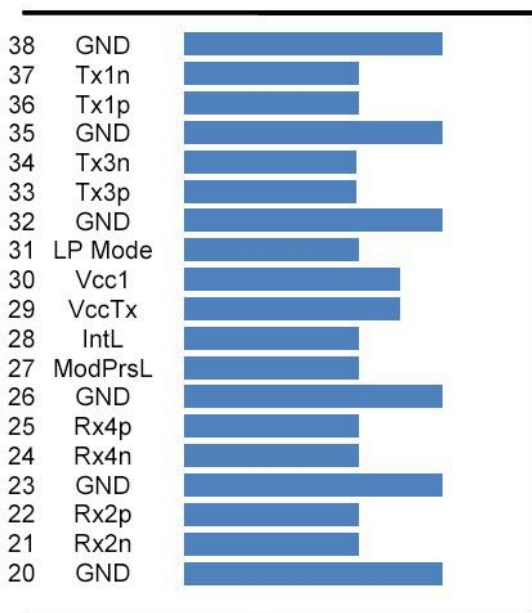
Note3: Measured with conformance test signal at receiver input for BER= 1×10^{-12} .



Transceiver Block Diagram

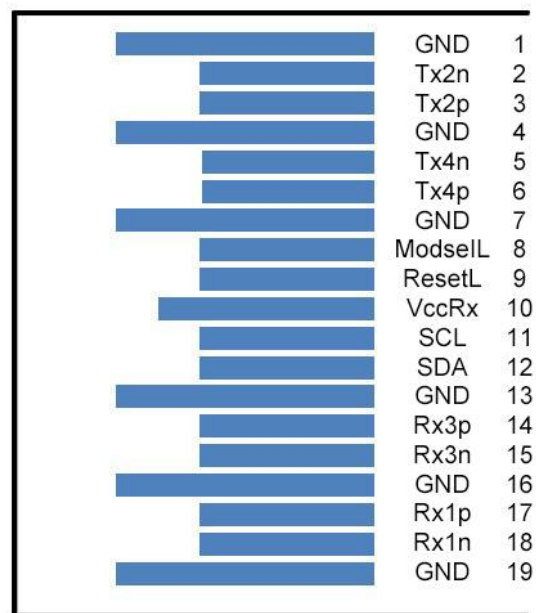


Pin Assignment



Top Side
Viewed From Top

Module Card Edge



Bottom Side
Viewed From Bottom



Pin Description

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMODE	Low Power Mode
32		GND	Module Ground

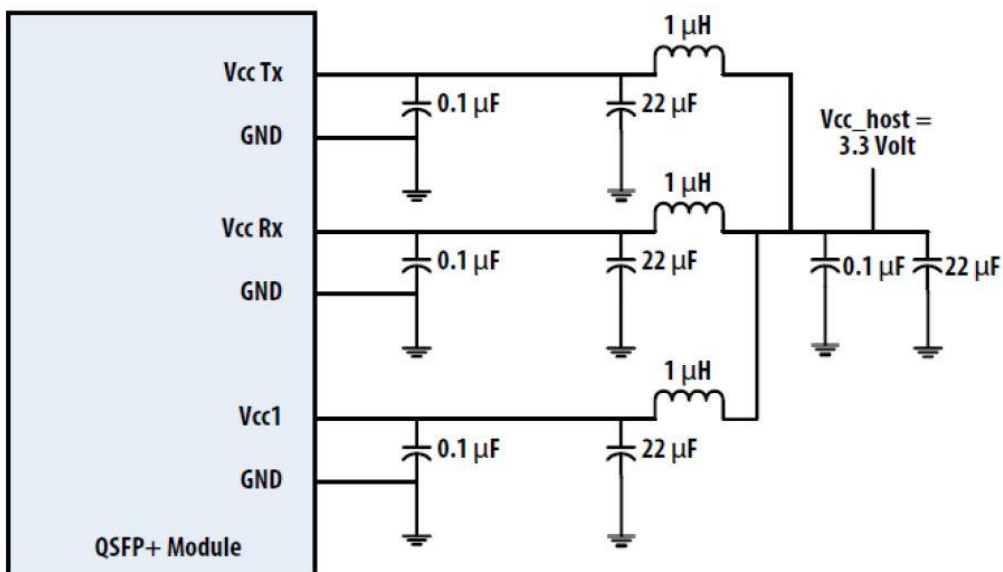


33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP+ modules. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Recommended Power Supply Filter





Digital Diagnostic Functions

As defined by the QSFP+ MSA, Ficer's QSFP28 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

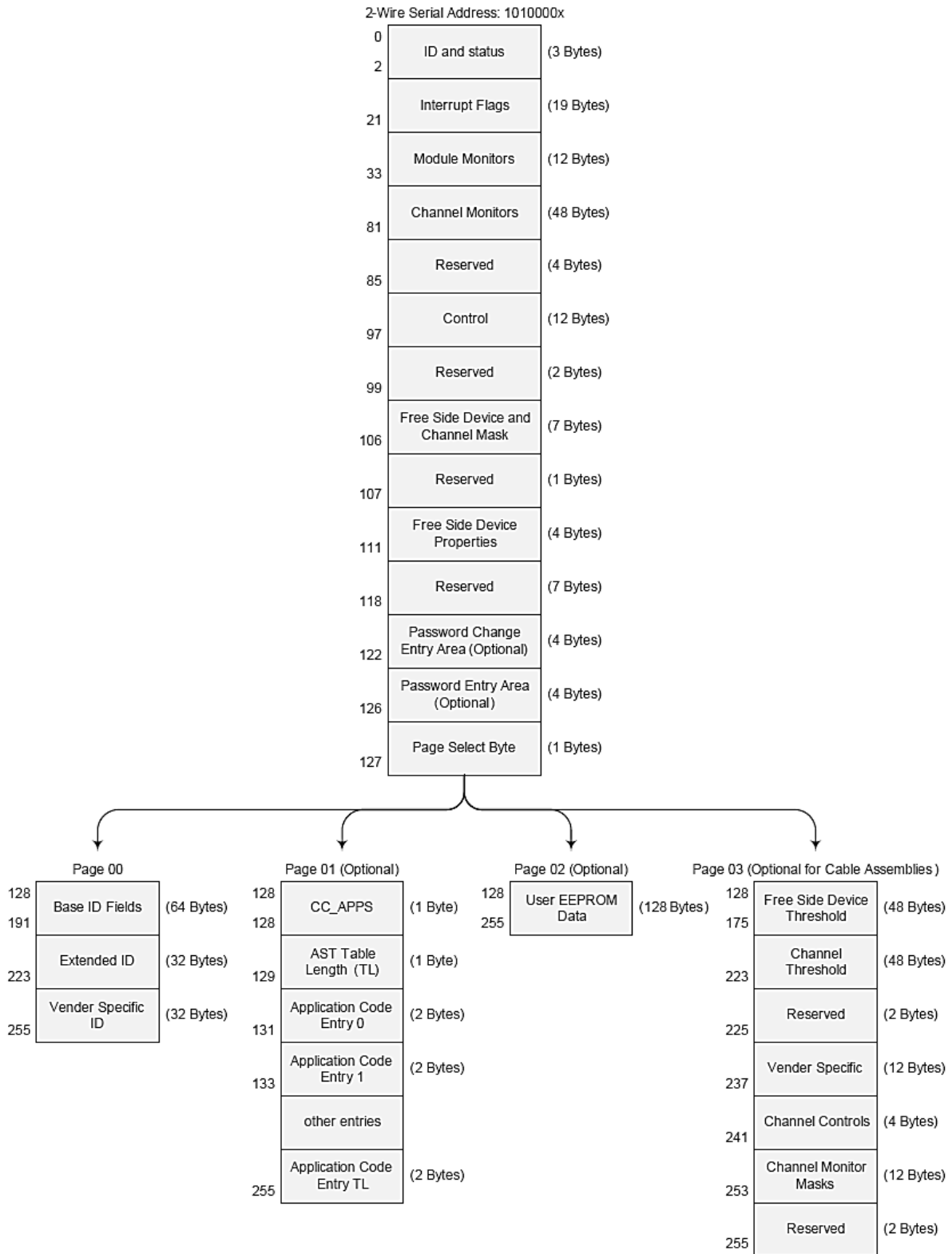
- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP+ transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

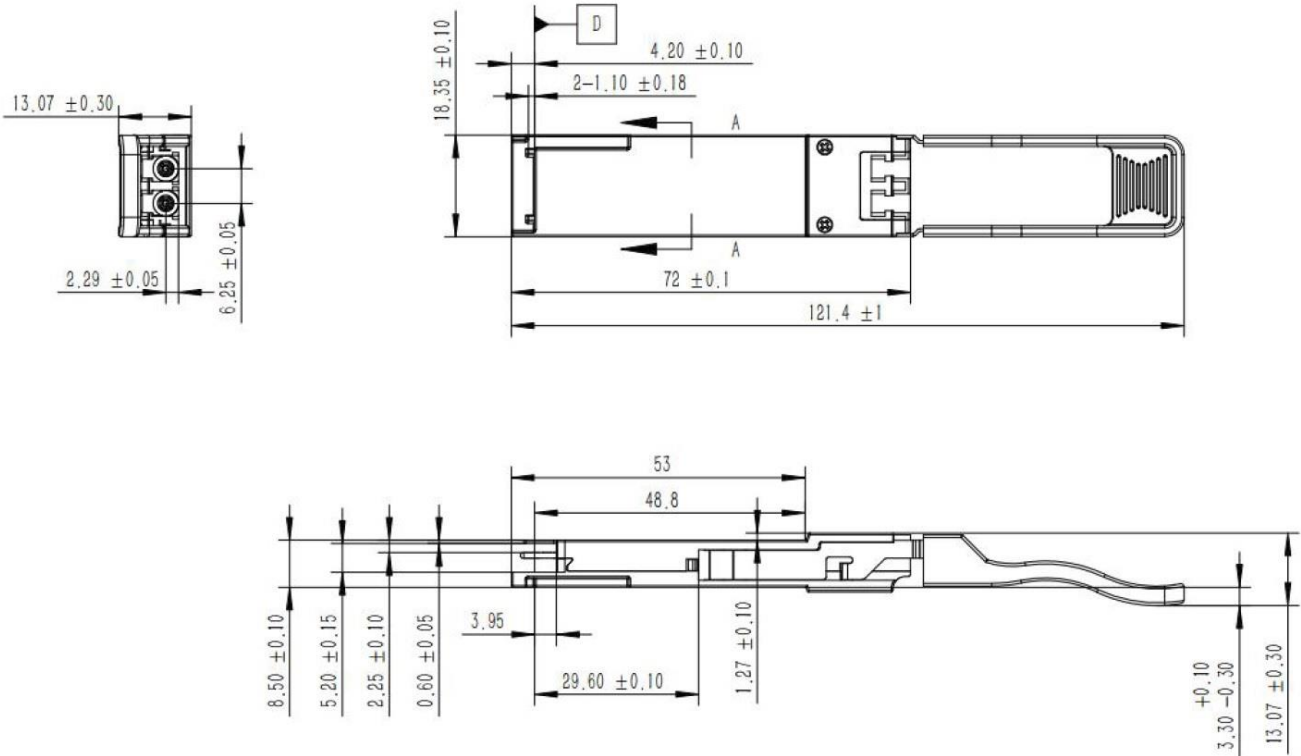
For more detailed information including memory map definitions, please see the QSFP+ MSA Specification.

Digital Diagnostic Memory Map





Mechanical Dimensions



(All Dimensions are ± 0.20 mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Tx	Rx	Link	DDM	Temp.
FQ28-K7-S85-X1D	850nm	850nm	MM OM3 75m	Yes	0~70°C
	880nm	880nm	MM OM4 100m		
	910nm	910nm	MM OM5 150m		
	940nm	940nm			

Note1: Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.